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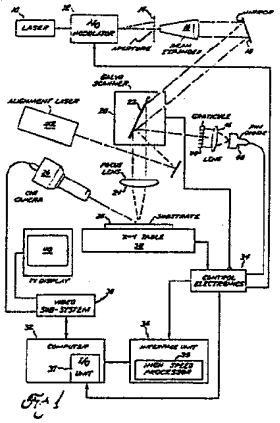
## (54) An adaptive lithography method and system.

(57) An adaptive method and system are disclosed for providing high density interconnections of very large scale integrated circuits on a substrate 28. The procedure is performed in four basic steps: first an artwork representation for the interconnections of the integrated circuits is generated. This artwork representation is stored in a computer data base and assumes the integrated circuits to be at predetermined ideal locations and positions on the substrate. Second, using imaging (26,38,40), the actual positions of each integrated circuit on the substrate are determined. The actual positions of the integrated circuits are compared with their ideal positions to compute an offset and rotation for each integrated circuit on the substrate. Third, the computed offsets and rotations are then used to modify the artwork representation stored in the data base to account for the actual locations and positions of the integrated circuits on the substrate. Finally, the modified artwork representation is used to drive a direct writing laser lithography system (10,12,16,18,20,22,24) that actually forms the high density interconnections of the integrated circuits on the substrate. The artwork representations are stored in computer data bases in vector form to minimize storage requirements. The laser beam produced by the lithography system is raster scanned on the substrate. Modulation of the laser beam is controlled by the real time conversion of the vector representation of the modified artwork to be a bit mapped representation. To assure accurate formations of the interconnects, a feedback alignment system (42,44,46,48) is used to accurately position the laser beam throughout its raster scan.



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**Description**

# AN ADAPTIVE LITHOGRAPHY METHOD AND SYSTEM

## Cross Reference to Related Applications

This application is related to the following copending applications by the present applicant, which are incorporated herein by reference:

"Method to Produce Via Holes in Polymer Dielectrics for Multiple Electronic Circuit Chip Packaging", PCT/US 87/02293, inventors Charles W. Eichelberger and Robert J. Wognarowski (General Electric docket RD-17,428).

"Integrated Circuit Packaging Configuration for Rapid Customized Design and Unique Test Capability", PCT/US 87/02497, inventors Charles W. Eichelberger, Kenneth B. Welles, II and Robert J. Wojnarowski (General Electric docket RD-17,431).

"Multichip Integrated Circuit Packaging Configuration and Method", PCT/US 87/02294, inventors Charles W. Eichelberger, Robert J. Wojnarowski and Kenneth B. Welles, II (General Electric docket RD-17,432).

"Method and Apparatus for Packaging Integrated Circuit Chips Employing a Polymer Film Overlay Layer", PCT/US 87/02501, inventors Charles W. Eichelberger, Robert J. Wojnarowski and Kenneth B. Welles, II (General Electric docket RD-17,433).

"Method and Configuration for Testing Electronic Circuits and Integrated Circuit Chips Using a Removable Overlay Layer" PCT/US 87/02473, inventors Charles W. Eichelberger, Robert J. Wojnarowski and Kenneth B. Welles, II (General Electric docket RD- 17,436).

The subject invention relates to a method and system for writing circuit patterns, e.g. with a focused laser beam and more particularly, to interconnecting integrated circuits.

The interconnection of pre-packaged circuit chips has been a principal means for the assembly of many electronic systems. In one such method, "the wire wrap method", sockets with wire wraps are provided and logic chips to be interconnected are placed in these sockets. Subsequently, interconnections are provided by wrapping wires around wire wrap pins according to a wire list. This can be done by automatic or manual machinery. The major drawback of wire wrap is the length of time required to wrap a single circuit board. This precludes this method from being economic for all but prototyping applications. In addition, wire wrapped boards cannot be checked for accuracy of wiring, both in interconnect ion accuracy and for shorts, except through the use of expensive, dedicated machinery. Also, wire wrap provides a relatively low performance interconnection since conductor runs are relatively long and since they also suffer from high capacitance loading effects. Also, once chips have been installed on a wire wrap board, it is difficult to partition the board for simple tests. Thus testing to the required high degree of functional assurance generally requires complex and time consuming testing apparatus. Finally, wire wrap prototyping boards are expensive because they contain a large number of holes and each wire wrap socket must supply long pins for wire wrapping.

Printed circuit boards are another method of interconnecting pre-packaged electronic circuit chips. A printed circuit board typically comprises copper runs adhered to an epoxy/glass fiber base substrate or the like. Packaged chips are mounted on the substrate and package pins are soldered to runs on the printed circuit board. In terms of phototyping, the time from completion of the circuit definition until populated boards (that is, boards with chips) are received can be quite long. Layout of printed circuit boards, if done by hand, can require two weeks to a month for a fairly complicated circuit board containing one hundred to two hundred chips. Even with computer aided layout, the amount of computer time required to route the board is substantial for a complicated board. In addition, complicated boards typically require multiple circuit layers which makes design and fabrication of printed circuit boards an even more time consuming process. A typical short turn around time can be on the order of two weeks. In addition, special tooling must be provided in order to test that all the connections are made on the board and that no undesired short circuits exist. At this point it is still necessary to populate the board with chips and to solder them in place. Chip population is generally done in different plant locations than board fabrication because a large number of chips must be kept in inventory and are specific to the needs of a particular operating department, while board fabrication is more generic in nature. The problem of testing the finished assembly is the same as with a wire wrap method in that a fully interconnected assembly generally requires a large array of complex test vectors (sample input patterns designed to exercise particular chip functions) in order to derive a high degree of assurance that the system will work under all desired conditions.

A gate array is also a solution to the problem of providing an electronic chip system. A gate array is primarily a medium to high volume device. In a typical gate array, arrays of P-channel and N-channel transistors are fabricated in an array structure on integrated circuit wafers. These circuits are generally completely fabricated with the exception of the last metallization step. Logic designs are achieved by custom connecting the P-channel and N-channel transistors with the last metallization layer. This method makes relatively efficient use of chip "real estate" and typically utilizes computer aided layout directly from circuit definitions. However, time is required to fabricate masks for the last metallization step and to finish the processing of the wafers. A typical time for the steps of automatic layout, mask generation and chip fabrication is generally at least two weeks. At this point, thousands of chips can be relatively easily fabricated, but thousands of chips are generally not required for prototyping quantities and for many applications. To further complicate the problem, complete

systems require custom testing by the vendor of the gate array with the test vectors and conditions developed and supplied by the circuit engineer. This must be done before the chips can be packaged. This means that the circuit engineer must carry out a sufficiently detailed simulation to develop a set of qualification test vectors. Further testing must be accomplished after prototype chips arrive at the circuit engineer's site. While simulation can greatly decrease the risk of design errors in the chips, it does not cover the operation of a chip in an electronic system substantially similar to its operating environment. Generally, faults will be found and updates will be necessary and the requirement for additional prototypes with more changes will be created. This process is both costly and stretches the time to completion of a project substantially because each iteration generally requires at least two weeks. In addition, a single gate array cannot provide all the structures necessary for a complete electronic system. For example, voltages and current may not be compatible at the interface level and may require addition of bipolar devices for analog-to-digital conversion at the input and digital-to-analog conversion at the output. Also, many systems require some form of memory. This means that the gate array would necessarily require an additional printed circuit board to interconnect the memory or interface devices.

A programmable logic array can be used to provide an electronic system economically in low volume for some applications. The major disadvantage of logic arrays is that they make inefficient use of silicon because the logic array must provide for all possible Boolean functions in "AND/OR" configurations. In those few applications where this type of Boolean logic is required, the logic array can be programmed for the desired Boolean functions. Most systems, however, require a large number of logic arrays to achieve the desired function and this is not economical except possibly for the very first prototype.

Fully customized integrated circuits can generally provide about two or three times the functionality available in the same area from a gate array, but the processing cost and non-recurring cost is substantially increased. Circuit layout involves all layers of the chip. Three month turn-around times are typical for the processing associated with a fully custom integrated circuit chip. Test vectors and probe cards are also unique to each application specific integrated circuit (ASIC) situation. This means that substantial number of chips must be involved before the fully custom chip is economical. As a rule of thumb, volumes over ten thousand units per year are generally required.

In the packaging of very large scale integrated (VLSI) circuit devices, a great deal of space is taken up by mechanisms for interconnecting one chip to an adjacent device. This makes the packaging of integrated circuit devices and electronic components based thereon larger than necessary. As a result of this, many individuals are involved in the development of so-called wafer-scale integration processes. However, efforts expended in these directions have generally tended to be limited by the problem of yield. Because a certain number of chips or dies on a wafer are often found to be defective, the number of wafers that are produced that are completely usable is generally lower than is desired. Furthermore, there still exists the problem of interconnecting the various chips on a wafer and the concomitant problem of testing a large system, such as results when a number of highly complicated individual integrated circuit components are interconnected. Accordingly, it would be very desirable to be able to construct wafer scale integrated circuit packages from individual, easily testable integrated circuit chips.

A slightly different problem also exists, as follows. In present day electronic systems, the primary components are usually readily available. These components include random access memory (RAM) and microprocessor chip family sets as well as analog-to-digital and digital-to-analog conversion chips. In present day systems, these primary components are interconnected using transistor-transistor logic (TTL). TTL logic refers to a set of functional blocks generally referred to as the 7400 series and is described in the handbook The TTL Data Book for Design Engineers published by Texas Instruments, Inc. This function of interconnecting, buffering and tying together the primary components of the system is generally referred to as a "glue logic function". For example, in present day integrated circuit boards, one often finds certain standard functional chips surrounded by a plurality of custom interconnected integrated circuit chips in familiar dual in-line packages (DIP packaging). It is these numerous small surrounding chips that provide a "glue function". In future systems, the glue logic function may be provided by gate arrays and custom chips where a single chip replaces a large number of TTL chips. This leads to several problems. The first is that the number of pins in the custom glue chip can be quite high. In addition, all of the primary components are immediately available. In the past, TTL was also immediately available and system interconnection could commence immediately on receipt of a given design. However, a time discontinuity now exists in which the primary components are available, but the custom glue logic takes many weeks to fabricate. The invention described in copending application PCT/US 87/02497 (General Electric docket RD-17,431) uses a generic glue logic chip which can be used in place of a large number of TTL logic chips.

In an encapsulating process, semiconductor chips are mounted on a substrate, and a layer of material such as polytetraflouroethylene (PTFE) is pressed over the tops of the chips and around the chips so that the chips are completely encapsulated in this layer. Holes are etched in the encapsulating layer corresponding to pad positions on the chips. Metallization is applied and patterned to form interconnections. However, in the process just described, known as semiconductor thermodielectric processing (STP), the chips are completely embedded in PTFE material so that no overlay layer as such exists. This makes it impossible to repair an assembly since the chips cannot be removed. Even if a chip could be removed, the remaining chips would still be encapsulated in the PTFE material and there would be no way to install a replacement chip. In addition, there is no provision in the semiconductor thermodielectric processing method for a removable metallization

layer which is selectively etched, thus protecting the underlying circuit while assuring complete removal of the metallization layer. In addition, the semiconductor thermodielectric processing method faces two other problems. First, by encapsulating chips in a polymer, a high degree of stress is created by difference in thermal expansion coefficients. Second, the thickness of the polymer over the top of the chips is governed solely by the thickness of the chip and the tooling which encapsulates the chips. Variations in chip thickness lead to variations in the thickness of the polymer over the chip.

As described in more detail in, for example, copending application PCT/US 87/02294 (General Electric docket RD-17,432) and PCT/US 87/02501 (General Electric docket RD-17,433), a multichip integrated circuit package may be produced by arranging a plurality of individual integrated circuit chips on a common substrate and then covering the chips on the substrate with a polymer film overlay layer or layers. The via holes are formed and metallized interconnections between the pads of the individual chips are provided. This packaging technique is, however, highly dependent on the precise and accurate placement of the chips on the substrate. What is needed, especially for automated packaging of integrated circuit chips, is a procedure which is less dependent on the highly accurate placement of the chips on the substrate.

According to the packaging technique of co-pending applications PCT/US 87/02294 (General Electric Docket RD-17432) and PCT/US 87/02501 (General Electric Docket RD-17433), a polymer film covers a plurality of integrated circuit chips adjacent to one another on an underlying substrate. Furthermore, the polymer film provides an insulative layer upon which a metallization pattern for interconnection of individual circuit chips is eventually deposited. The method of disposing a polymer film over a plurality of integrated circuit chips affixed to an underlying substrate is described in copending application PCT/US 87/02501 (General Electric docket RD-17,433). The inventions disclosed therein solve significant problems with respect to high temperature processing and the requirement for excellent compliance of a plastic material to an irregular surface. The chips include interconnection pads for connecting to other integrated circuit components or for connecting to other parts of the same chip. Via openings or apertures in the polymer dielectric layer are aligned with the interconnection pads. The pattern of interconnection conductors is disposed on the overlying polymer film so as to extend between at least some of the via openings so as to provide electrical connections between various parts of a chip or between several chips. The method for producing via holes in polymer dielectrics for multiple electronic circuit chip packaging is described in copending application PCT/US 87/02293 (General Electric docket RD-17,428).

Metallization is preferably provided by sputtering a one thousand angstrom thick layer of titanium, followed by a one micron thick layer of copper over the polymer film and into the via holes. The metallization is preferably patterned by spraying or spinning a coating of photoresist on the copper surface, drying for about one half hour at approximately 90° C and exposing the positive resist material with a scanned ultraviolet (UV) laser beam under control of computerized artwork. A preferable photoresist material is Dynachem OFPR 800 photoresist.

To promote speed, interconnection from one chip to another is preferably accomplished with a minimum of capacitative loading and a minimum of interconnect length. Capacitative loading tends to slow down signal transmission such that high speeds attained on the chip cannot be maintained in communicating from one chip to another. Interconnection length between chips also contributes to propagation delay due to greater capacitative loading effects in the dielectric medium due to circuit length and also due to a self inductance of the interconnection circuit. The metallization is patterned to form very fine lines and spaces, typically under 1 mil (25μm) in line width and 1 mil (25μm) in line spacing. Copending application PCT/US 87/02294 (General Electric docket RD-17,432) describes the ability to interconnect chips placed edge to edge because the metallization pitch is much finer than the pad spacing.

Commercially available chip placement devices are not sufficiently accurate to position chips with the resolution capability of a laser scan system.

The present invention interconnects integrated circuits which are not accurately placed by first identifying the actual position of each chip and subsequently adapting interconnection and via patterns to conform to the actual chip positions. The term "artwork" is often used and refers to such patterns in the form of a database which describes interconnect structure and via hole structure for providing interconnects between electronic components.

A lithography system embodying the invention adapts to inaccurately placed chips by modifying database artwork patterns represented an ideal interconnect pattern so as to accommodate the actual position of integrated circuit chips. The modified artwork may provide information to drive a focused laser beam under computer control to directly write circuit patterns in metallization and photo resist.

An aspect of this invention provides a method for modifying artwork representing an ideal interconnect pattern to accommodate the actual position of the integrated circuit chips. The four major steps of the method are: generating artwork patterns for the ideal case, determining the actual positions of each integrated circuit component, modifying the artwork to match the actual chip positions, and using the modified artwork to produce the desired effects in adaptive lithography scanning system. The packaging technique of copending applications PCT/US 87/02294 (General Electric Docket RD-17432) and and PCT/US 87/02501 (General Electric Docket RD-17433) also incorporates a packaging system and method in which polymer film overlays are provided with metallization patterns as a means for configuring an integrated circuit chip or chips in an operating arrangement.

Preferably artwork is generated for the ideal positioning of integrated circuit chips using a computer-aided

layout system. All interconnect, via hole definitions, and chip boundary definitions are created in a file. The chip boundary definitions include an outline of a chip and an outline of the extend to which the chip can be misplaced. The actual positions of the integrated circuit components are determined from via hole and chip outline information. Ideally, this process is performed automatically by using a charge-injection device (CID) camera and an image recognition technique to align each circuit chip and calculate offset and rotation information. In the process actually implemented and described hereinafter, the process is partly manual.

More specifically, in an embodiment of the present invention the substrate is aligned on an x-y table in both location and rotation according to fiducial marks on the substrate. The monitor for the CID camera is equipped with a bull's-eye or cross-hair pattern on the center of the screen. When the fiducial mark on the substrate which corresponds to the mirror zero position is near the bull's eye, the x and y position counters are reset to zero. The computer then supplies pulses to x and y stepping motors to step to the ideal position of the upper right hand pad of the integrated circuit chip. A mouse connected to the computer is used to move the image of one pad of the actual chip directly under the cross- hairs. The difference between the actual position and the ideal position is recorded. Then the computer steps the x-y table to the expected position of a pad on the opposite side of the integrated circuit chip, making the assumption that the chip is not rotated from the ideal position. The mouse is used again to position the image of the actual pad directly under the cross hairs. Again, the difference between the actual position and the ideal position is recorded. The offset and rotation of the actual chip is then recorded from the results of the two operations. The computer then goes to the next chip in sequence and determines its offset and rotation and this process is repeated until the offset and rotation of all the chips have been recorded. The information determined during this step is stored in a database which defines the chip positions. The ideal artwork is modified to match the actual chip position. All of the interconnect patterns and associated via holes are modified to incorporate the offset and rotation associated with each integrated circuit chip. The modified artwork is used to drive the adaptive lithography scanning system. The modified artwork is used to supply the commands for positioning the x-y table and to supply data to the high speed processor for driving the adaptive lithography scanning system and for modulating the laser beam so that a modified printed circuit pattern can be printed on the substrate.

The structure of the adaptive lithography system includes a primary laser beam path which starts from an Argon ion laser which is adjusted with optics to provide ultraviolet (UV) output. The laser provides a single beam which may be divided, with beam splitting optics, into as many beams as are required. The laser beam is then passed through an acousto-optical modulator which deflects the beam when a high frequency signal is applied. A plate with an aperture is positioned approximately one meter from the output of the modulator. The non-deflected beam is stopped by the plate and the deflected beam passes through the aperture.

The deflected beam is expanded to the desired diameter laser beam with a beam expander. The expanded beam is directed to a galvanometer driven scanner which has a (9-millimeter) diameter scanning mirror and an internal sensor which is coupled with a servo-amplifier to accurately position the mirror. The scanned beam is focused onto a substrate with a conventional plano-convex lens. A second laser is used to accurately determine the position of the scanning mirror at all times during the scan. The second laser beam is passed through a graticule and focused on a PIN diode detector.

A CID camera with a microscope objective is mounted to observe the area on the substrate where the laser beam focuses. Precise correlation between the laser beam position and the image of the CID camera is obtained. The substrate is positioned on a precision x-y table, which is positioned by precision screws attached to separate motors. The CID camera is connected to a video subsystem which drives a television display.

A microcomputer, such as a MS-DOS personal computer (PC), manages the process and dataflow. An input/output board connects special control electronics which manage the motion of the x-y table to the PC. The image data from the CID camera is sent through an interface board to a high speed processor which generates bit map patterns of the artwork stored in vector form. The control electronics for the adaptive lithography system can be divided into three major sections which are: x- y table control, mirror scan control, and laser data control. Circuitry is included which assures that the x-y table is in exact synchronism with the position of the scanning mirror. The lithography system operates by converting a file stored in rectangular vector form to a controlled flow of data which modulates a laser beam in synchronism with its position on the substrate to be exposed.

The system can be expanded to achieve higher throughput rates at a substantial savings by duplicating only essential parts of the device. The system can be duplicated as many times as required to obtain the desired throughput rate. The acousto-optic modulator, the expander, the scanner, and the focus lens as well as the alignment laser and graticule must be duplicated. The x-y table, the CID camera, the PC, and other equipment need not be duplicated.

An adaptive lithography system according to the present invention may be provided which is particularly attractive because it requires few processing steps. Also, the time to produce photomasks and the yield and deterioration problems are eliminated. If desired, the direct writing system is able to customize each circuit produced.

It can be seen that an embodiment of this invention provides a direct writing lithography system for direct laser exposure of positive or negative photoresist.

Also, an embodiment of the invention may provide a direct writing lithography system which can provide commercial through-put rates but which exposes photoresist at allowable power densities.

Further, an embodiment of the present invention may provide a direct writing lithography system which can accommodate the interconnection of chips with an accuracy which is an order of magnitude higher than chip placement accuracy.

An embodiment of the invention may provide a system which can easily produce customized devices.

Additionally, an embodiment of the present invention may provide a direct writing lithography system which requires a minimum of memory to store the image data by computing, in real time, an image-vector-data-base to bit-map conversion.

A preferred embodiment of the invention may provide a direct writing lithography stem which achieves higher resolution than implied by scanning mirror drift and jitter.

A preferred embodiment of the invention may provide a direct writing lithography system which incorporates acceleration and deceleration of an x-y table, along with speed and position control such that continuous table motion can be obtained with higher accuracy than available from commercial grade table screws.

An embodiment of the present invention given by way of non-limiting example, will now be described with reference to the accompanying drawings, in which:

Figure 1 is a block diagram of an adaptive lithography system embodying with the present invention;
Figure 2 is a block diagram of an x-y table drive and position sensor;
Figures 3A and 3B are circuit diagrams for the control electronics;
Figure 4 is a graphical representation of start-run and stop-timing of the system;
Figure 5 is a graphical representation of mirror scan and pixel clock timing;
Figure 6 is a graphical representation of timing of the x-y table synchronized to the mirror scan;
Figure 7 is a plan view of ideal artwork;
Figure 8 is a plan view of modified artwork; and
Figure 9 is a block diagram of an adaptive lithography system showing the portions to be duplicated for multiple substrates.

Copending application PCT/US 87/02501 (General Electric docket RD-17,433) describes a method and apparatus for applying a removable polymer overlay layer. Copending application PCT/US 87/02293 (General Electric RD-17,428) describes a preferred method for supplying the overlay layer with a pattern of apertures for connection to interconnect pads located on integrated circuit chips. Copending application PCT/US 87/02294 (General Electric docket RD- 17,432) describes a method for providing a preferred form of metallization patterning over a polymer film. Details of a preferred laser exposure system are disclosed in copending application PCT/US 87/02293 (General Electric docket RD-17,428).

Referring now to the drawings and, more particularly, to Figure 1, a laser 10 such as an Argon ion laser is adjusted with optics for an output of approximately 0.4 watt in the ultraviolet (UV) range. Laser 10 may be a Spectra Physics 2505 unit. The laser beam is passed through acousto-optical modulator (A/O) 12 to plate 14 with an aperture. The modulator deflects the beam when a high frequency signal is applied to the modulator. Acousto-optical modulator 12 may be a Newport Optics Systems Quartz Modulator. An undeflected beam is stopped by plate 14 positioned approximately one meter from acousto-optical modulator 12, while a deflected beam passes through the aperture to beam expander 16 which expands the laser beam in accordance with the diffraction limits to achieve a desired eight micron focussed laser spot. The beam expander used may be an Oriel Model 1510. UV-grade aluminum coated mirror 18 is used to deflect the expanded beam into proper alignment with galvanometer driven scanner 20. The scanner used may be a General Scanning 120 D.C. galvanometer scanner. Scanner 20 preferably has a nine millimeter diameter scanning mirror 22 and an internal sensor which can be coupled with a servo-amplifier for accurate positioning. The scanned beam is focused with plano-convex lens 24 having a focal length of one hundred millimeters onto substrate 28. CID camera 26 with a microscope objective is mounted to observe the area on substrate 28 where the laser beam is focussed. The CID camera used may be a General Electric Model TN 2505A2. Substrate 28 is placed on precision x-y table 30 which is positioned by precision screws 102 (see in Figure 2), attached to separate motors 101 and 103 (also see Figure 2). Precision x-y table 30 may be the type supplied by New England Affiliated Technologies. Computer 32 manages the dataflow in the adaptive lithography system. The computer used may be an IBM PC/XT. Control electronics 34 which control the motion of x-y table 30 are connected to computer 32 by input/output board 37. Input/output board 37 may be of the type made by Techmar. Interface board 36 interfaces high speed processor 35 with computer 32. Interface board 36 may be a Sky 320 PC board made by Sky Computers of Lowell, Massachusetts, which contain high speed processor 35 chip, such as TMS 320- 10 chip made by Texas Instruments. High speed processor 35 is used to generate bit map patterns from artwork stored in vector form and to process image data from CID camera 26. CID camera 26 is connected to video subsystem 38 which drives television display 40 and communicates with computer 32. Video subsystem 38 used may be a Data Translation DT2803 unit. The position of scanning mirror 18 is accurately determined with the use of an alignment laser 42. Alignment laser 42 may, for example, comprise a 0.5 milliwatt helium neon laser from Spectra Physics. Alignment laser 42 emits a beam which is deflected by scanning mirror 22 and passed through graticule 44. The beam is then focussed by a lens 46 onto PIN diode detector 48.

Figure 2 shows details of the x-y table drive and position sensing, as well as a map of raster scan pattern 100 traced by the beam from laser 10. Separate stepper motors 103 and 104 drive precision screws 102 to position x-y table 30. Drive electronics 105 and 106 receive pulsed information from control circuitry 114 and 116 and then translate the information into stepping x-y table 30 by stepper motors 103 and 104 to the desired location. Linear encoders 108 and 110 attached to the edges of x-y table 30 encode the table position to a resolution of

one micron with a standard format two-phase, ninety degree square wave pattern 112. Phase A ($\varphi_A$) always transitions before phase B ($\varphi_B$). Circuitry 114 and 116 decode the motion and direction of motion of the table 30. Circuits which can detect motion and direction of motion are well known in the art. For example, Bausch and Lomb supplies a decoding circuit for use with their linear scales which features digital readout in microinches and microns called the Accurite Quick Count II. An up/down counter provides a binary value which corresponds to the number of microns moved. A reset signal is used to zero the up/down counter and, thereby, to establish a reference point. After zeroing, all positions are measured relative to the position of the x-y table 30 where the up/down counter was reset. The scanning mirror scans back and forth deflecting the laser beam on the x-axis in a saw tooth pattern; that is, the scan progresses from left to right for a period of approximately one and a half milliseconds, then quickly returns to the left most position in half a millisecond. Each scan covers a distance of approximately six millimeters. As the laser is scanned in a direction on the x-axis by scanning mirror 22, table 30 is moved at a constant speed in a direction on the y-axis. When the laser beam reaches the edge of x-y table 30, x-y table 30 is moved to the right six millimeters and then begins to move at a constant rate in the opposite direction on the y-axis.

The mirror scan and table movement are synchronized so that the laser spot is accurately positioned. Figures 3A and 3B show a detailed block diagram of the control electronics used in one embodiment of an adaptive lithography system. The control is divided into three sections, which are: x-y table control, mirror scan control, and laser data control. The x-control portion is accomplished by the x position sensor in circuitry 114 being connected to an input port in the computer 32. Pulses are supplied from computer 32 to drive electronics 106 for x-direction stepping motor 104. The output of the x position sensor is compared in the computer 32 with the desired x position. Pulses are again supplied by the computer 32 to the stepper motor 104. The cycle is continued until the desired x position and the actual x position match within plus or minus one micron. The y position control has a mode identical to the x position control in which the computer 32 controls the position accuracy, but it also has a mode in which x-y table 30 is scanned at a fixed speed in synchronism with scanning mirror 22. The circuit is configured to operate in a self-standing mode, controlling acceleration, speed synchronization, and deceleration so that computer 32 is free to oversee the high speed data transfer of the image data for the patterns. Five words of data are supplied which represent specific y positions for x-y table 30, these are: base (a base position), edge 1 (the first edge of the substrate), edge 2 (the opposite edge of the substrate), slow (the position where deceleration should begin), and stop (the position where the x-y table 30 should stop). This data is written to random access memory (RAM) 210 by clearing address counter 212 and clocking address counter 212 from computer 32. For each new address, data is applied to the RAM 210 and then a write pulse is supplied. When the data has been written, address counter 212 is cleared to the first address and multiplexor 214 is switched such that the address counter clock is supplied from the output of comparator 216. Comparator 216 compares the present y position and the position stored in RAM 210 at the location addressed by address counter 212. The first address location would be the base y position. When the actual y position is the same as that stored in RAM 210, a pulse is issued from comparator 216. This pulse clocks address counter 212 to the next storage location in the RAM 210. Decoder circuit 218 is connected to the address and clocked by comparator 216. As a result, the base, edge 1, edge 2, slow, and stop locations are identified for use by appropriate control circuitry. Scanning is started when a pulse is issued from computer 32 to SR flip-flop 220. The output of flip-flop 220 is connected to integrator 222 whose output is connected to voltage controlled oscillator (VCO) 224. The output of VCO 224 is connected to y drive electronics 105 for controlling stepping motor 103. The result of the arrangement is that as integrator 222 integrates up, the voltage of VCO 224 is increased, and a stepping motor accelerates x-y table 30.

The start-run and stop-timing of the system is shown in Figure 4. It is understood that as integrator 222 continues to integrate, it eventually reaches a voltage greater than the voltage set by resistive divider 226 consisting of resistors R-1 and R-2. At this point diode D1 is cut off and the voltage to VCO 224 no longer rises. The speed of x-y table 30 then remains essentially fixed with x-y table 30 continuing to move at essentially constant speed until the slow position stored in RAM 210 is traversed. The slow pulse resets flip-flop 220, and integrator 222 integrates downward. VCO 224 decreases the speed of stepper motor 103 at a fixed ramp rate. When the stop position is traversed, a pulse is issued to flip-flop 228 which then completely disables VCO 224 and, therefore, no further pulses are sent to drive electronics 105. Additional circuitry provided in the x-y control allows synchronization of the x-y table position with the mirror scan. This circuitry is connected to provide a vernier adjustment of the approximately constant speed voltage provided to VCO 224 by resistor divider 226.

The mirror scan control (see Figure 3B) provides a basic scan signal to mirror 22, and a vernier adjustment of that scan signal so that the time to traverse a particular angle exactly matches the desired scan rate. In addition, a circuit is provided for very accurately determining the position of the mirror during the active data portion of the scan and for supplying clock pulses to clock data to laser modulator 12 such that the data supplied corresponds exactly to the position of the laser spot on the substrate being exposed.

Figure 5 shows a timing diagram for the important waveforms shown in the mirror scan control circuit. The basic position drive is derived from counter 230 which counts pulses from master clock 231 and outputs the count to a digital-to-analog converter 232. The output from digital-to-analog 232 converter is a sawtooth waveform and is the mirror drive signal. The period of the sawtooth is directly related to master clock 231 which is used for timing synchronization throughout the scan control system. In the embodiment illustrated, counter 230 overflows when the count reached is 2,048 and then counter 230 starts over again at zero. The mirror drive

signal is applied to mirror servo circuit 234 which provides a drive to galvanometer mirror scanning device 20. Galvanometer device 20 is equipped with a position sensor which feeds back information to the mirror servo circuit 234 to allow the mirror to be quickly driven to positions directly corresponding to the mirror drive signal. Unfortunately, there is drift in the mirror position sensor and there is jitter in the position of the mirror 22 caused by bearing fluctuations. These effects cause the mirror position to be only approximate and not generally repeatable relative to the high level of accuracy required in the adaptive lithography system. For this reason, alignment laser 42 is directed at scanning mirror 22 and the reflected alignment beam is passed through graticule 44 and focused on PIN diode 48. The output signal from PIN diode 48 is amplified by amplifier 235, filtered by filter 236, and thresholded by threshold detector 238 to provide a square wave signal which is exactly representative of the angular position of scanning mirror 22. Graticule 44 consists of opaque lines and clear spaces. The edges of the square wave signal output correspond to the edges of graticule 44. Graticule 44 contains fewer lines by a factor of ten than the number of pixels which must be scanned by mirror 22 onto substrate 28 over the corresponding angle. Ideally, a one-for-one correspondence would be desired. Unfortunately, alignment laser 42 cannot be focused sufficiently well on graticule 44. Thus, a very low-level, unreliable signal otherwise would result which is highly dependent on dust particles and other contaminants landing on graticule 44. Pulse circuit differentiator 240 receives the output of threshold detector 238 to create a pulse on each edge; that is, from black to clear as well as from clear to black, for use by the rest of the circuitry. The graticule signal and corresponding graticule pulses are shown in Figure 5. Flip-flop 242 enables counter 244 at the time when counter 230 reaches a preset count which is chosen so that counter 244 is enabled slightly in advance of the sweeping of the main laser beam over the area to be exposed. The J input to flip-flop 246 is also enabled so that when the first graticule pulse occurs, flip-flop 246 is set and counter 248 is enabled. Counter 248 subsequently counts a preset number of master clock pulses before its output resets flip-flop 246. During this same interval, counter 244 counts a preset number of graticule pulses before its output resets flip-flop 242. The outputs of flip-flop 242 and flip-flop 246 are compared in a phase comparator circuit 250. The output of phase comparator circuit 250 drives amplifier 252 that provides a vernier control voltage to digital-to-analog converter 232 providing the mirror drive signal. Therefore, the angle of mirror 22 is controlled so that a fixed number of graticule pulses occurs during a fixed number of master clock pulses. As a result, the speed of mirror 22, while it is scanning the area on substrate 28 to be exposed, is synchronized to master clock 231. A drift in the mirror position servo circuit 234 is automatically compensated by this vernier control circuitry.

Unfortunately, mirror jitter, which is essentially a noise quantity, can cause the mirror to deviate more than one pixel element away from its ideal location. To eliminate this effect, the circuitry of counters 254 and 256, in conjunction with the graticule pulses, generates a pixel clock signal which is precisely related to the actual position of mirror 22. Counter 254 is clocked by master clock 231 and is enabled by flip-flop 246. Counter 256 is cleared by flip-flop 258. Flip-flop 258 is set by graticule pulses and reset by the output of counter 256. After counter 254 reaches a present count, its output causes a pulse to be issued. Counter 254 pulses are combined with the graticule signal pulses to form the pixel clock. This circuit portion works as follows: whenever a graticule signal occurs, counter 254 begins counting the master clock pulses; each time counter 254 overflows, a pulse is issued to the pixel clock; counter 256 counts the pixel clock and when nine pixel clock pulses have occurred, flip-flop 258 is reset; counter 254 and counter 256 are both cleared and must wait until another signal occurs; when another graticule signal occurs, a new pixel clock signal is issued. In this way, nine pulses equally spaced, occur in response to each graticule signal. An additional pulse, which is the tenth pulse in the series, is coincident with the graticule signal and is provided by pulse block 260. Hence the pixel clock is locked to the graticule signal. The graticule signal indicates the exact position of the scanning mirror 22 while there are ten time as many pixel clocks as there are graticule signal transitions. The pixel clock is used to identify each pixel position which is scanned by the laser.

The laser data control circuitry shown in Figures 3A and 3B indicates that high speed processor 35 is incorporated in the computer system using an interface board 36. A section of memory is shared between computer 32 and interface board 36. Data is stored on a Winchester type disk in computer 32 in vector format such that each rectangle to be written is given an x minimum, a y minimum, an x maximum, and a y maximum. Vectors describe a line as two points. These two vectors then define any rectangle. A series of bits called a bit map is generated to turn the laser beam on and off as it scans substrate 28. High speed processor 35 calculates the bit map from the vector rectangle data. Only a small section of the total area to be scanned is covered by the bit map; in this embodiment of the invention a section which is 1,024 pixels wide by 256 pixels long is computed and stored. The 1,024 pixels correspond directly to the width of the active scan area scanned by scanning mirror 22, and the 256 pixel length corresponds to the y motion of the table which occurs during the 256 sequential scans of the mirror 22. High speed processor 35 processes the sorted vector data and places it in one section of pingpong memory and subsequently sets up direct memory access pointers such that data is supplied sequentially from the pingpong memory whenever it is requested by the control electronics. A pingpong memory is one that has data read out of one half of the memory, as data is loaded into the other half. In the meantime, high speed processor 35 calculates the next set of 1,024 by 256 points and places this set in the second half of the pingpong memory. When the first half of the pingpong memory is exhausted, the direct memory access pointers are set to the other half, and high speed processor 35 begins computing the next bit map in order. Data is transferred from high speed processor 35 in 16-bit words. The data transfer process begins when flip-flop 260 is set by the first edge signal. This occurs when the first edge

of substrate 28 to be scanned is directly under the laser scanning beam. Flip-flop 262 synchronizes this event with the x window signal which indicates that scanning mirror 22 is at the start of its scan position. At this point, word counter 268 and the requisite flip-flop 264 are reset. Word counter 268 begins to count pixel clocks and when eight pixel clocks have occurred, word counter 268 clocks flip-flop 264 which makes a request for data to the direct memory access circuitry of high speed processor 35. Data is supplied from high speed processor 35 to latch circuit 266 with a data acknowledged signal. Data is latched to latch circuit 266 and flip-flop 264 is reset. When sixteen pixel clocks have occurred word counter 268 indicates a pulse which loads data from latch circuit 266 to shift register 270. The output of shift register 270 is supplied to laser modulator 12. By this method, data is continuously supplied to shift register 270 and clocked by the pixel clock to modulate laser 10 with the appropriate data for the exact position of the laser beam on substrate 28 to be exposed. When the far edge of the substrate is reached, the far edge signal resets flip-flop 260 and the next x window signal clocks flip-flop 262 which holds word counter 268 and flip-flop 264 in their inactive states.

The circuitry to accomplish synchronism between x-y table 30 and scanning mirror 22 is shown in Figures 3A and 3B in the x-y table control section. While x-y table 30 is accelerating at its nominal speed, up/down counter 272 is held in its zero position by the output of flip-flop 274. When x-y table 30 reaches the y base position flip-flop 274 is set, up/down counter 272 is enabled, and up pulses are supplied to up/down counter 272 from counter 276 which is clocked by master clock 231. Counter 276 is reset by x window pulse such that output pulses from counter 276 are synchronized with the x window. The count for counter 276 is chosen so that six outputs occur for each x window pulse. This is because x-y table 30 travels six microns between sequential scans of scanning mirror 22. Down pulses are supplied to up/down counter 272 from y-position sensor 116 on x-y table 30. Counter 272 remains at the zero position if the number of up pulses equals the number of down pulses. If more of one pulse than the other occurs, up/down counter 272 accumulates the pulses so that the output of digital-to-analog converter 278, connected to up/down counter 272 provides a voltage correction to VCO 224 to either increase or decrease the number of pulses to stepping motor 105 and, thereby, to bring x-y table 30 motion back into synchronism with the mirror position. Flip-flop 280 enables the y-move pulses to be supplied to up/down counter 272. When the base signal occurs, flip-flop 280 is reset and y move pulses are not applied to the up/down counter 272. Flip-flop 10 is subsequently set by the x window transition indicating the beginning of the scan to scan mirror 22. Up pulses from counter 276 are accumulated in up/down counter 272 over the period from the occurrence of the y-base signal until the occurrence of the x-window signal. In this way, although there are six microns between each scan of the scanning mirror 22, the exact micron desired, as identified by y base, is forced to correspond to the starting of the mirror scan as identified by the rise of the x-window signal. Figure 6 shows the timing thus described where it is shown that up/down counter 272 accumulates from the onset of the y base signal to the rise of the x-window signal. At this point, the servo circuitry forces coincidence between x-y table 30 position and the counts synchronized to the x-window signal such that up/down counter 272 averages to zero with only plus or minus one count discrepancy. This means that x-y table 30 is held at speed to within one micron of the exact desired position corresponding to scanning mirror 22.

The operation of the adaptive lithography system has been explained in terms of converting a file stored in rectangular vector form to a controlled flow of data which modulates a laser beam in synchronism with its exact position on substrate 28 to be exposed. If all components could be positioned to sufficient accuracy, the laser could scan a fixed pattern of interconnect wiring. However, commercially available chip placement devices are not sufficiently accurate to position chips within the resolution capability of a laser scan system. Therefore, a method is provided for modifying artwork representing an ideal interconnect pattern to accommodate the actual position of the integrated circuit chips. The four major steps required are: generating artwork for the ideal case, determining the actual positions of each integrated circuit component, modifying the artwork to match the actual chip positions, and using the modified artwork to drive the adaptive lithography scanning system.

Ideal case artwork can be generated using a computer aided layout system or an automatic routing system. The article entitled "End-to-End Design" by Richard Angell on pages 97 to 119 of the November 1986 issue of PC Tech Journal describes the PCB-3 design system from P-CAD for generating and converting electronic schematics through placement and routing of printed circuit boards. The article entitled "PC Board Layout Via AutoCAD®" by Charles Jubb on pages 51 to 59 of the Volume 1, Number 2 issue of Cadence discusses overlay programs of the AutoCAD® software package from Autodesk, Inc.. An implementation of this invention uses an AutoCAD® printed circuit layout device which allows various layers to be defined according to user selected spacing and user selected line width. The AutoCAD® system runs on various microcomputers with a mouse input device to define the extent and position of the interconnecting lines. The AutoCAD® system outputs a document exchange file (DXF) which contains a hierarchical structured definition of the artwork according to each layer. Listing 1 in Appendix A shows a portion of a DXF file. In the hierarchy, a block which defines the outline of each integrated circuit chip can be defined. Figure 7 shows a portion of a simple interconnect pattern between the outlines 300 of several integrated circuits. An interconnect layer and a via layer shows the via interconnections from the conductors to pads on the chips. A second outline 310 marks the limit of the extent to which the chip can be misplaced. The second outline 310 can be changed depending on the positioning equipment used. The DXF file is stripped of its hierarchy in a process referred to as levelling so that the various important pieces of information can be used by other programs in adaptive lithography system. Levelling creates all interconnect, via hole definitions, and chip

boundary definitions according to a known format. Any computer aided design (CAD) system can interface to the adaptive lithography system with only changes in the software which convert to the stripped level of data coding being necessary.

Via hole and chip outline information are used to find the actual positions of each electronic component in the system. Ideally, this process is performed automatically with CID camera 26 using image recognition techniques to align each component and calculate offset and rotation information. The process as actually implemented, however, is at this time partially manual. The substrates are first aligned on the x-y table 30 in terms of position and rotation according to fiducial marks on substrates 28 by observing a television monitor 40 which displays an image from CID camera 26. Television monitor 40 is equipped with a bull's eye or cross hair pattern on the center of the screen. When the fiducial mark on substrate 28 which corresponds to the zero position of mirror 22, is under the cross hairs, the x and y position counters, indicated by control circuitry 114 and 116 in Figure 2, are reset to zero. Computer 32 now supplies pulses to x and y stepping motors, 104 and 103, respectively, to step to the ideal position of the upper right hand pad of the first integrated circuit chip. A mouse input device connected to computer 32 is used to move on pad of the actual chip directly under the cross hairs. The difference between the actual position and the ideal position is recorded. Next, computer 32 steps x-y table 30 to the expected position of a pad on the opposite side of the chip, making the assumption that the chip is not rotated from the ideal position. The mouse is then used to position the pad directly under the cross hairs. At this point, it is possible to compute both offset and rotation of the chip. Computer 32 then steps x-y table 30 to the next chip in the sequence with the process being repeated until the position and rotational offsets of all chips have been recorded. The information gathered is stored in a data base which defines the chip positions.

The ideal artwork generated in the first step and shown in Figure 7 is then modified to match the actual chip position as shown in Figure 8. Note that there are three distinct areas in this modified artwork. The first area is the interconnect pattern outside of second outline 310 which defines the degree to which the chip can be misplaced. In the first area the interconnect pattern is unchanged from the ideal case. The second area is the area that overlies integrated circuit chip outline 300 which defines the boundaries of the integrated circuit chip in question. All of the interconnect pattern and associated via holes are modified to incorporate the offset and rotation associated with the given integrated circuit chip. The third area is the area between the integrated circuit chip outline 300 and the second outline 310 defining the limit of misplacement of the chip. In this area interconnects which cross the boundary start from an unchanged position and end at the positions which are changed in offset and rotation according to the actual position of the chip.

The modified artwork is then used to supply the routines which position x-y table 30 and supply data to high speed processor 35 for the purpose of driving the adaptive lithography scanning system and modulating the laser beam to "paint" the appropriate modified pattern on the substrate to be exposed.

To obtain the desired throughput rate, the system can be duplicated as many times as required. Figure 9 shows the parts of the system which should be duplicated separated from the parts of the system which can be shared. The duplicatable parts are enclosed in a dotted block. Beam splitter 400 is positioned in front of the laser 10 to divide the single beam laser into as many beams as are required. Typically an input power of 0.2 watts is sufficient to expose photoresist. This is easily accomplished by dividing a 2 watt laser into ten beams. A substantial cost savings results from sharing x-y table 30, computer 32, CID camera 26, television display 40, video subsystem 38, alignment laser 42, and graticule 44, as well as dust elimination equipment and housing facilities. Acousto-optic modulator 12, beam expander 16, galvanometer scanner 20, and focus lens 24 must be duplicated for each laser beam. However, x-y table 30 and CID camera 26 need not be duplicated because all substrates 28 to be scanned can be mounted on a single table and only one CID camera is necessary to determine the position of each substrate 28. High speed processor 35 with latches and chip registers which drive the acousto-optic modulator 12 are also required for each substrate 28 so that the artwork for th substrate 28 can be converted from rectangle vector form to bit map form in real time.

While the invention has been described in detail herein in accord with certain preferred embodiments thereof, many modifications and changes therein may be effected by those skilled in the art.

# APPENDIX A

## Listing 1

```
  2
SETVIEW
  2
MERGE2
  9
$ACADVER
  1
AC1.50
  9
  9
$EXTMIN
 10
0.0
 20
0.0
  9
$EXTMAX
 10
50.8
 20
52.324
  9
$LIMMIN
 10
0.0
 20
0.0
  9
$LIMMAX
 10
50.8
 20
50.8
  9
$VIEWCTR
 10
45.32445141
 20
25.5
  9
$VIEWSIZE
 40
51.0
  0
INSERT
  8
MT1
  2
ICLS167
 10
3.0
 20
9.188
  0
INSERT
  8
MT1
  2
ICLS167
 10
3.0
 20
12.188
  0
TRACE
  8
MT1
 10
0.5
 20
19.375
 11
0.5
 21
18.125
 12
1.75
 22
19.375
 12
1.75
 22
18.125
  0
TRACE
  8
MT1
 10
0.5
 20
16.875
 11
0.5
 21
15.625
 12
1.75
 22
16.875
 12
1.75
 22
15.625
  0
POINT
  8
DR1
 10
3.088
 20
1.317
  0
ENDBLK
  0
ENDSEC
  0
EOF
```

## Claims

1. An adaptive method for providing high density interconnections of integrated circuits on a substrate, said method comprising the steps of:
generating an artwork representation for the interconnections of said integrated circuits at predetermined ideal positions on said substrate;
determining the actual positions of each of said integrated circuits on said substrate;
modifying said artwork representation for the interconnections to match the actual positions of at least one of said integrated circuits; and
forming high density interconnections of said integrated circuits using said modified artwork representation.

2. The method according to claim 1 wherein said predetermined ideal locations and positions are stored in a first data base and the step of generating an artwork representation comprises the steps of:
providing a printed circuit layout of metallized conducting paths from a list of pin connections for said integrated circuits; and
storing a representation of said printed circuit layout in a second data base describing an interconnection structure for providing said high density interconnections.

3. The method according to claim 2 wherein the step for storing is performed by storing a vector representation of said printed circuit layout in said second data base.

4. The method according to claim 2 or Claim 3 wherein the step of determining comprises the steps of:
aligning an image of each of said integrated circuits in an image field of said substrate;
comparing each of said images of said integrated circuits with said predetermined ideal locations and positions and said integrated circuits on said substrate; and
calculating an offset and rotation for each of said integrated circuits based on said comparing step.

5. The method according to claim 4 wherein said step of aligning includes the step of generating a third data base describing the actual locations of predetermined features of each of said integrated circuit with respect to said substrate and wherein said step of comparing compares said first and third data base entries.

6. The method according to claim 5 wherein said modifying step comprises the step of altering said second data base according to calculated offsets and rotations for each of said integrated circuits to produce a fourth data base storing a vector representation of the modified artwork.

7. The method according to claim 6 wherein said forming step is performed by the steps of:
converting the vector representation of the modified artwork in said fourth data base to a bit mapped representation of said modified artwork; and
controlling a raster scanned laser beam in a metallized circuit forming system with said bit mapped representation of said modified artwork.

8. An adaptive lithography system for providing high density interconnections of integrated circuits on a substrate, said system comprising:
memory means for storing in a first data base an artwork representation for the interconnections of said integrated circuits at predetermined ideal locations and positions on said substrate;
imaging means for determining the actual locations and positions of each of said integrated circuits on said substrate;
computing means responsive to said memory means and said imaging means for modifying said artwork representation to match the actual locations and positions of each of said integrated circuits and to store, in a second data base in said memory means, a modified artwork representation; and
laser lithography means controlled by said modified artwork representation in said second data base for forming high density interconnections of said integrated circuits.

9. The adaptive lithography system according to claim 8 wherein the representations in said first and second data bases are vector representations, said system further comprising conversion means for converting the vector representation in said second data base to a bit mapped representation used to control said laser lithography means.

10. The adaptive lithography system according to claim 9 wherein said laser lithography means comprises:
a direct writing laser producing a laser beam;
scanning means for scanning said laser beam in a raster on said substrate; and
modulating means responsive to said bit mapped representation for modulating said laser beam as it is raster scanned on said substrate so as to define said interconnections according to said modified artwork reprepresentation.

11. The adaptive lithography system according to claim 10 further comprising alignment means for accurately determining the position of said scanning means at all times during scanning, said computing means being responsive to said alignment means for controlling said scanning means to accurately position said laser beam at points as it is raster scanned on said substrate.

12. The adaptive lithography system according to claim 11 wherein said scanning means comprises:
deflecting means for deflecting said laser beam in a first direction; and
displacement means carrying said substrate for displacing said substrate in at least a second direction at an angle to said first direction; and wherein said alignment means comprises:
an alignment laser, graticule and photodiode, said alignment laser producing a light beam deflected by said deflecting means the deflection of which is sensed by said graticule and photodiode; and
computing means being responsive to said photodiode and said imaging means.

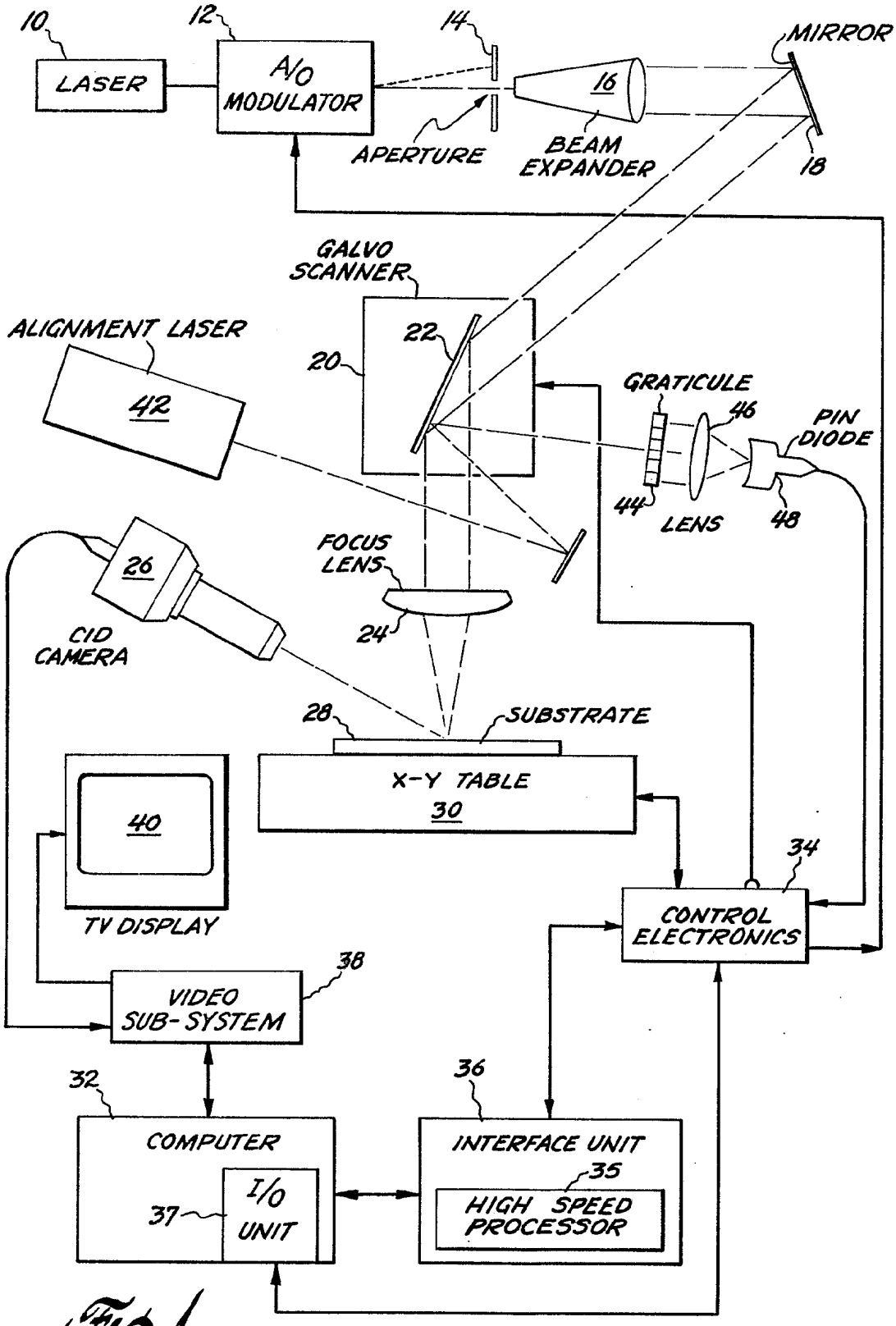

10
LASER
12
A/O MODULATOR
14
APERTURE
16
BEAM EXPANDER
MIRROR
18
GALVO SCANNER
20
22
ALIGNMENT LASER
42
GRATICULE
44
46
LENS
PIN DIODE
48
26
CID CAMERA
FOCUS LENS
24
28
SUBSTRATE
X-Y TABLE
30
40
TV DISPLAY
34
CONTROL ELECTRONICS
38
VIDEO SUB-SYSTEM
32
COMPUTER
37
I/O UNIT
36
INTERFACE UNIT
35
HIGH SPEED PROCESSOR

Fig. 1

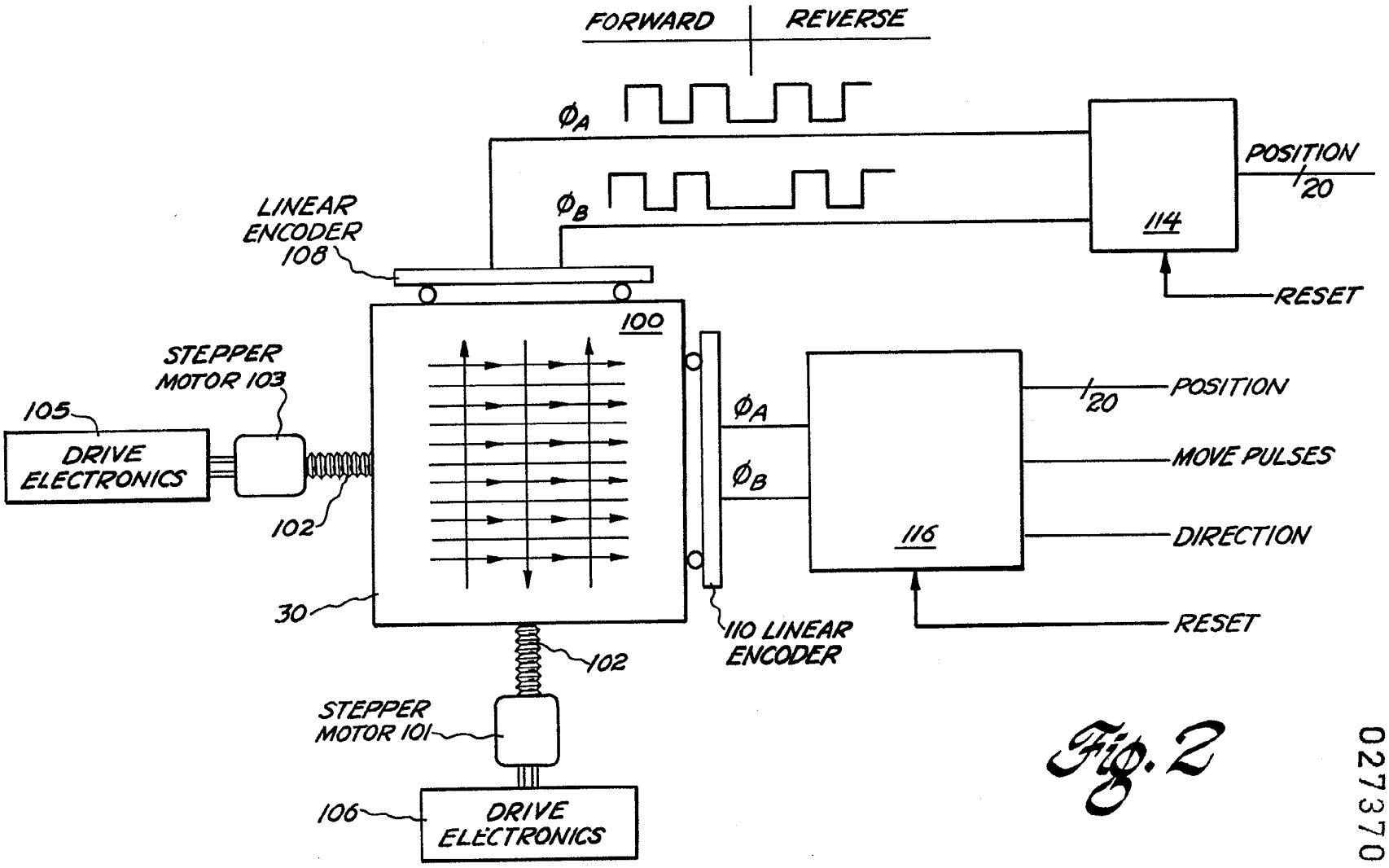



Fig. 2

0273703

Fig. 3A(1)

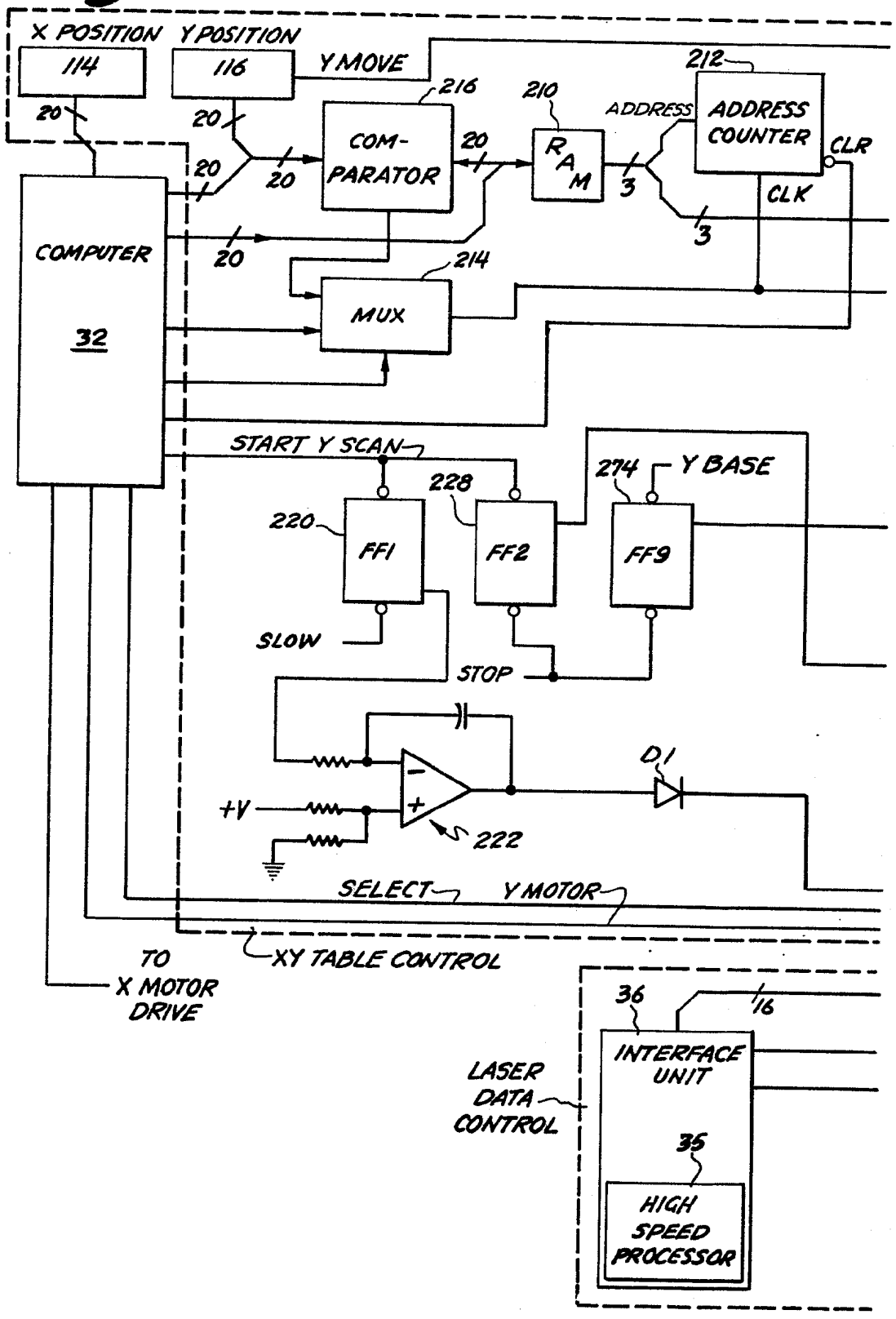

X POSITION
114
Y POSITION
116
Y MOVE
20
20
20
20
20
COM-
PARATOR
216
20
210
RAM
ADDRESS
212
ADDRESS
COUNTER
CLR
CLK
3
3
COMPUTER
32
20
MUX
214
START Y SCAN
228
220
FF1
FF2
274
Y BASE
FF9
SLOW
STOP
D1
+V
222
SELECT
Y MOTOR
XY TABLE CONTROL
TO
X MOTOR
DRIVE
36
16
INTERFACE
UNIT
LASER
DATA
CONTROL
35
HIGH
SPEED
PROCESSOR

Fig. 3A(2)

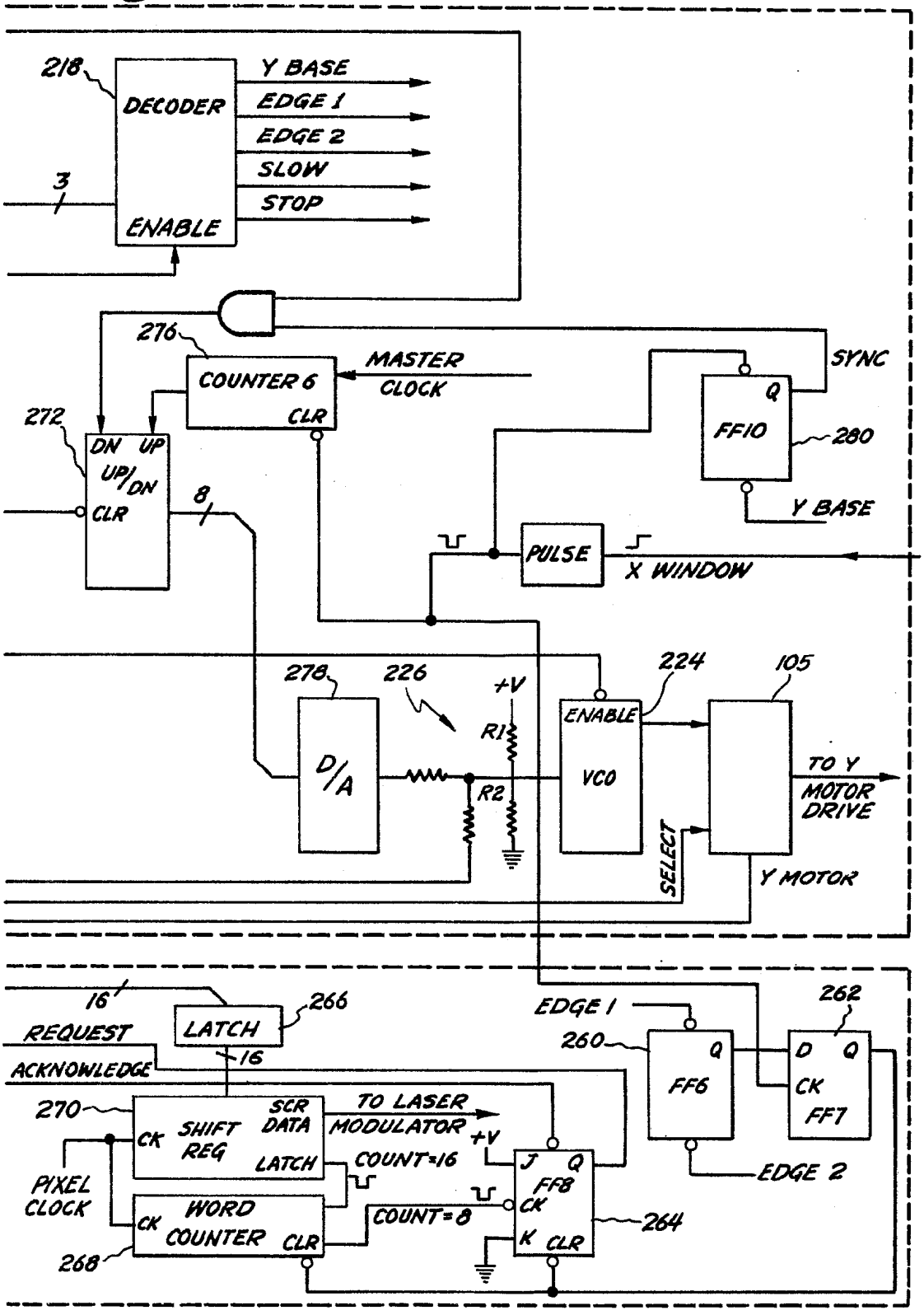

218
DECODER
Y BASE
EDGE 1
EDGE 2
SLOW
STOP
3
ENABLE
276
COUNTER 6
CLR
MASTER CLOCK
SYNC
Q
FF10
280
Y BASE
272
DN UP
UP/DN
CLR
8
PULSE
X WINDOW
278
226
+V
R1
R2
D/A
ENABLE
VCO
224
105
TO Y MOTOR DRIVE
SELECT
Y MOTOR
16
REQUEST
ACKNOWLEDGE
LATCH
266
16
270
CK
SHIFT REG
SCR DATA
LATCH
TO LASER MODULATOR
+V
COUNT=16
PIXEL CLOCK
CK
WORD COUNTER
CLR
COUNT=8
268
J Q
FF8
CK
K CLR
264
EDGE 1
260
Q
FF6
262
D Q
CK
FF7
EDGE 2

Fig. 3B

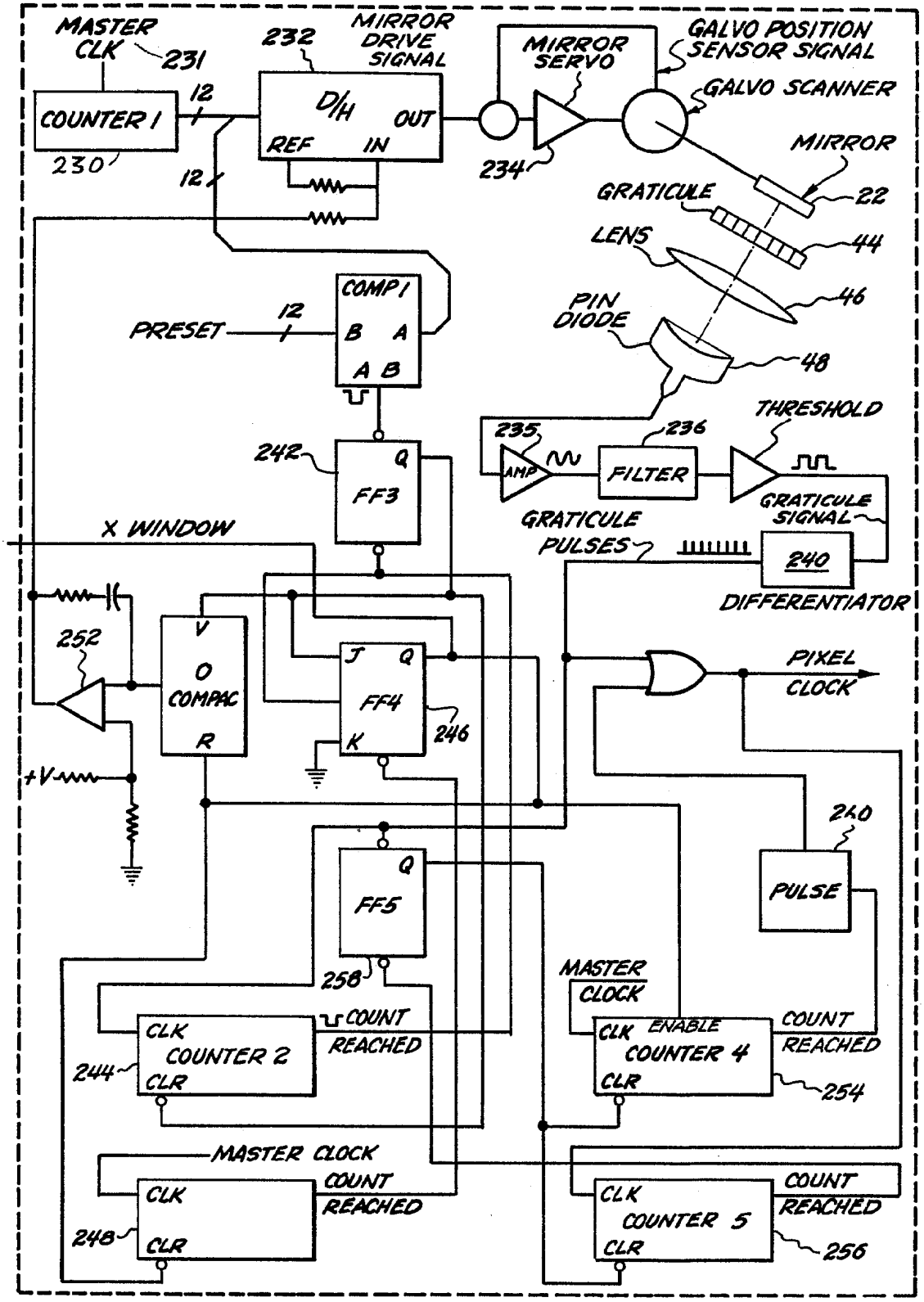

MASTER CLK
231
COUNTER 1
230
12
232
MIRROR DRIVE SIGNAL
D/H
REF
IN
OUT
12
MIRROR SERVO
234
GALVO POSITION SENSOR SIGNAL
GALVO SCANNER
MIRROR
22
GRATICULE
44
LENS
46
PIN DIODE
48
COMP 1
PRESET
12
B A
A B
242
Q
FF3
235
AMP
236
FILTER
THRESHOLD
GRATICULE SIGNAL
GRATICULE PULSES
240
DIFFERENTIATOR
X WINDOW
252
V
O
COMPAC
R
J Q
FF4
K
246
+V
PIXEL CLOCK
Q
FF5
258
240
PULSE
MASTER CLOCK
CLK
COUNTER 2
CLR
244
COUNT REACHED
CLK ENABLE
COUNTER 4
CLR
254
MASTER CLOCK
CLK
CLR
248
COUNT REACHED
CLK
COUNTER 5
CLR
256

Fig. 4

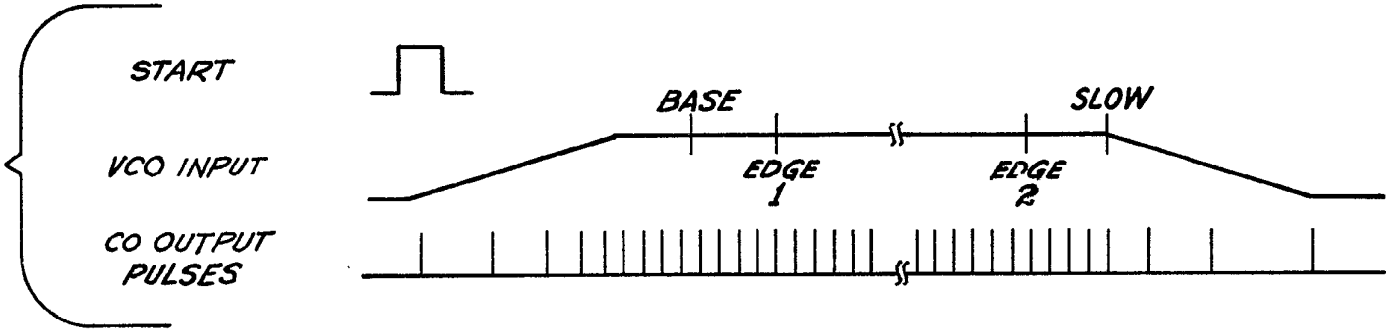



Fig. 6

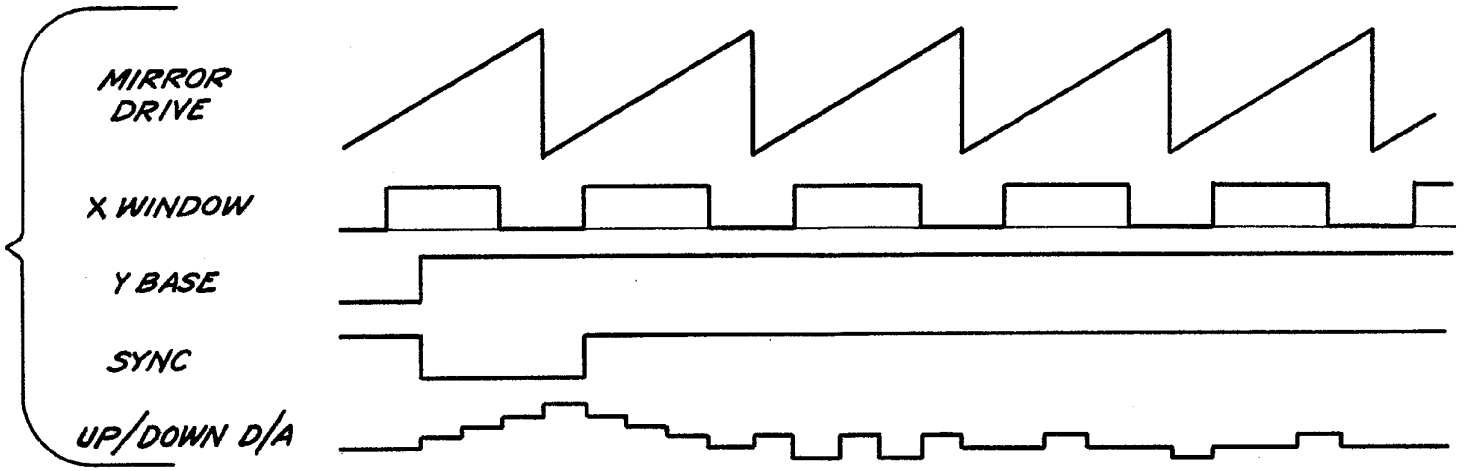
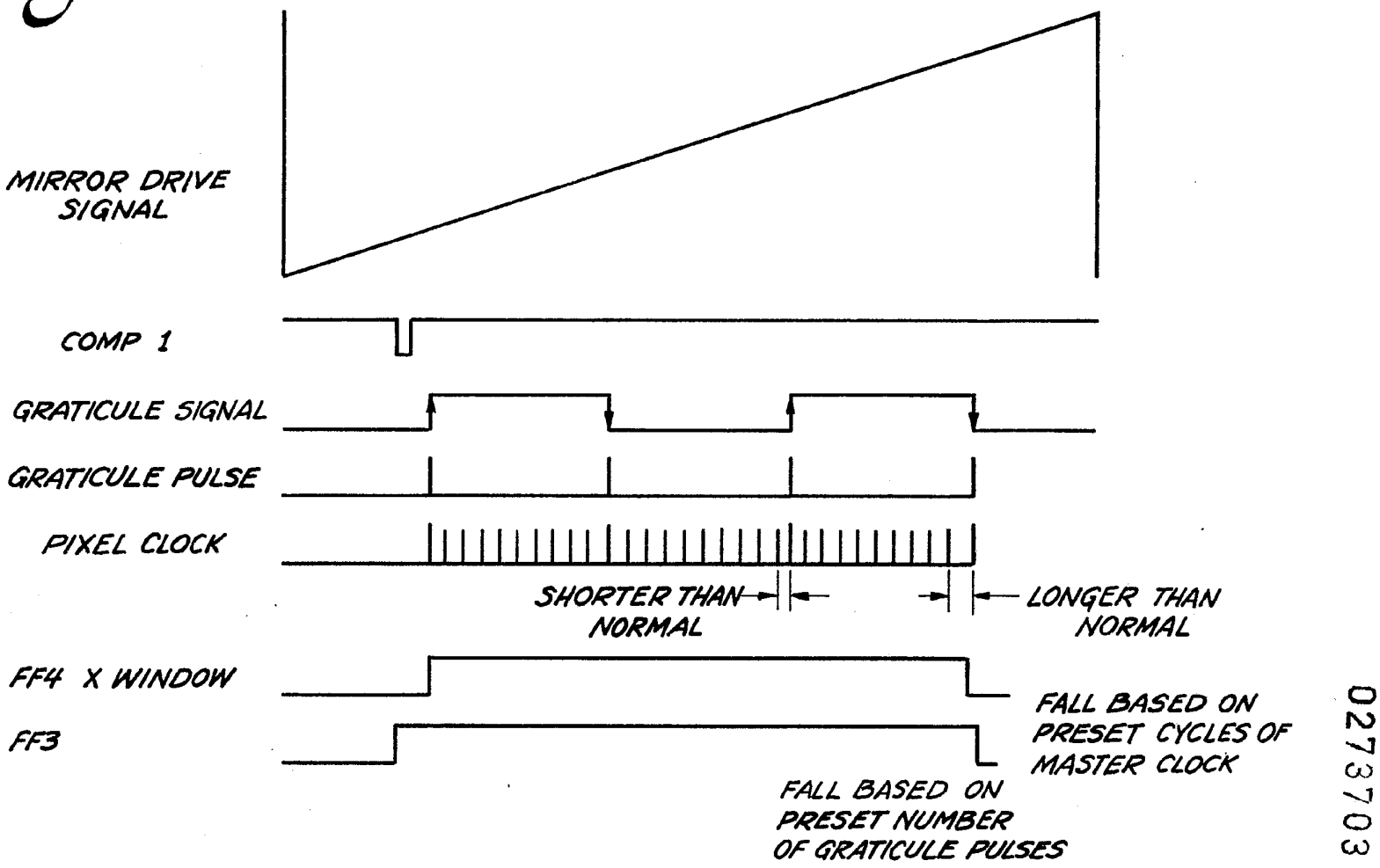


Fig. 5



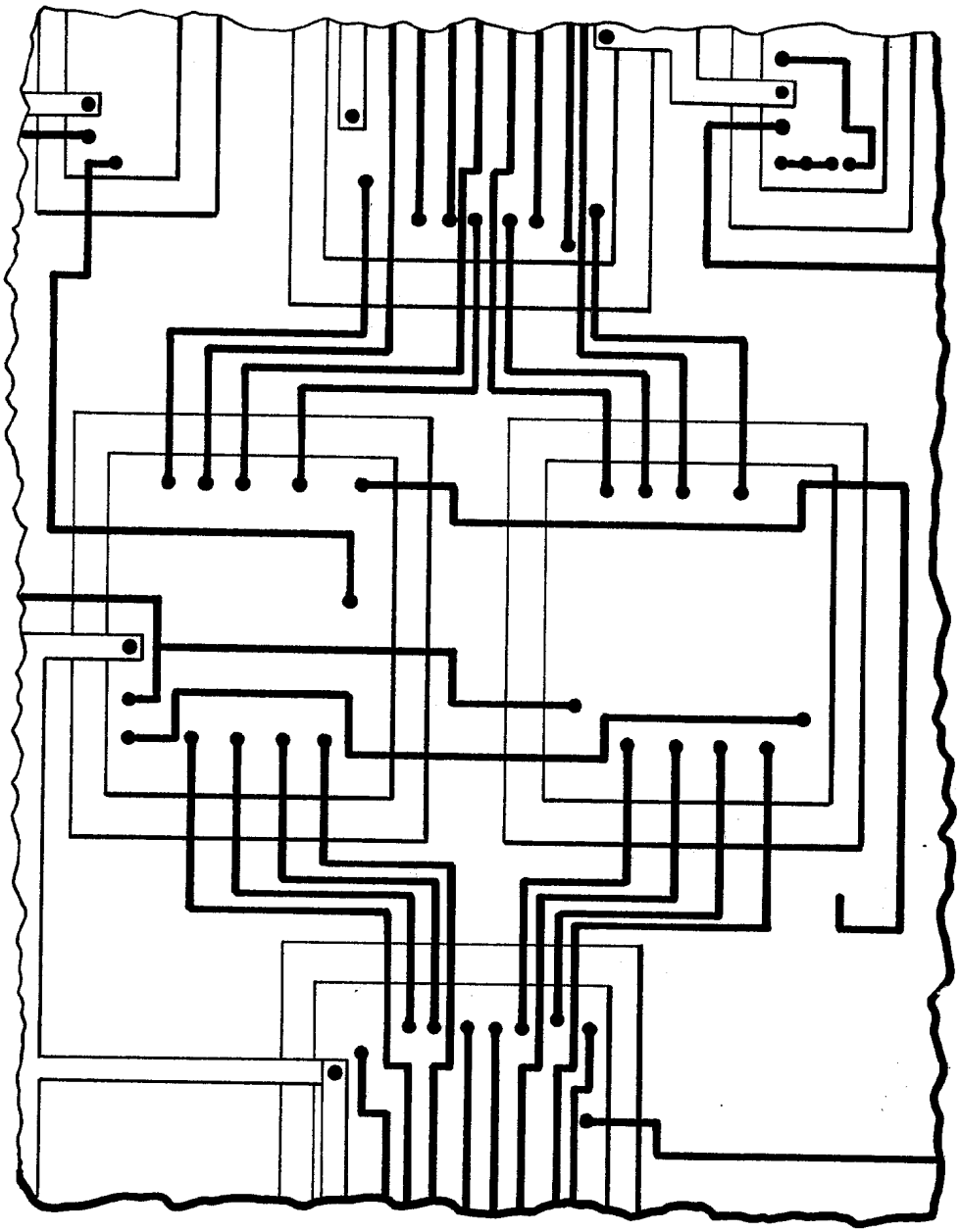


Fig. 7

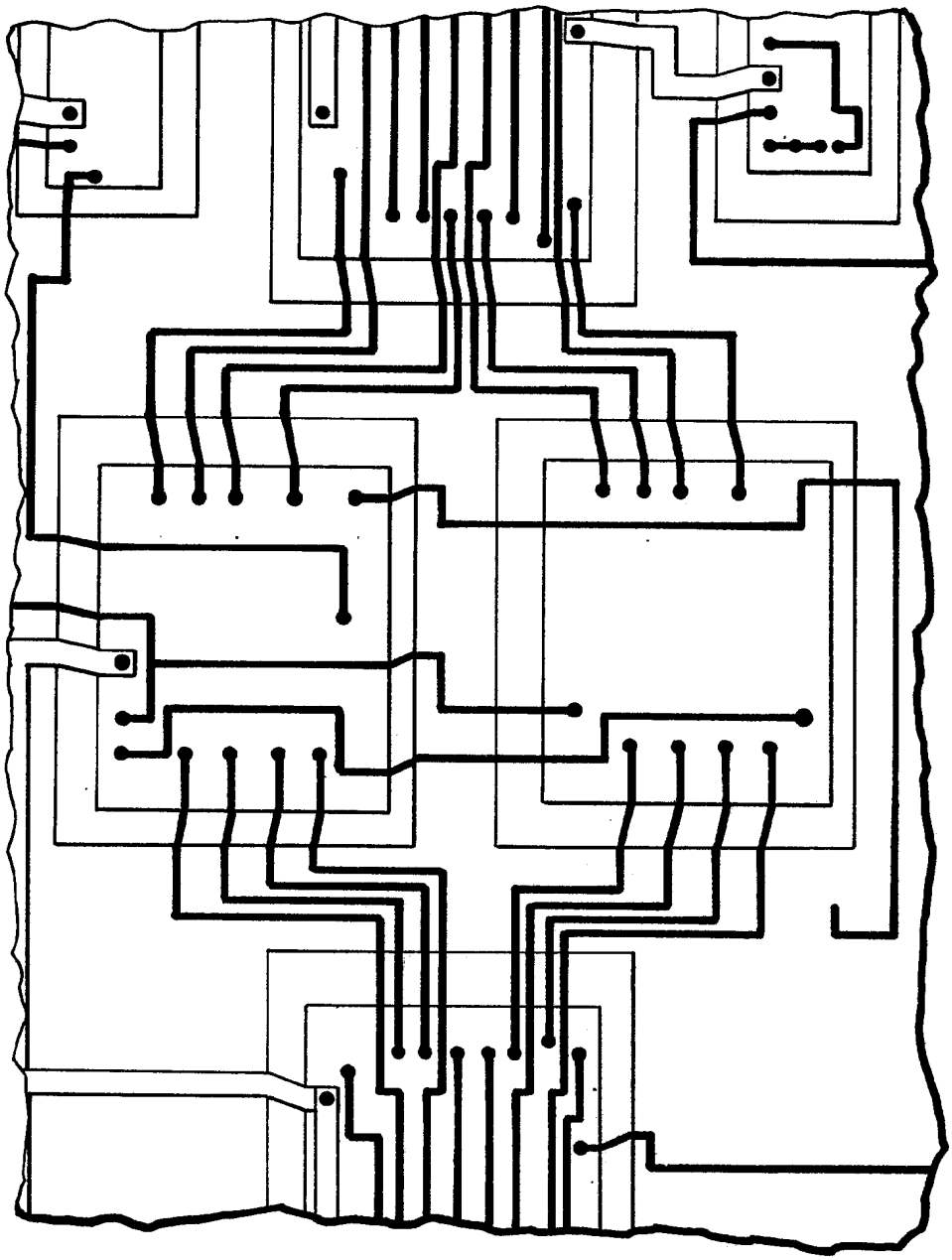
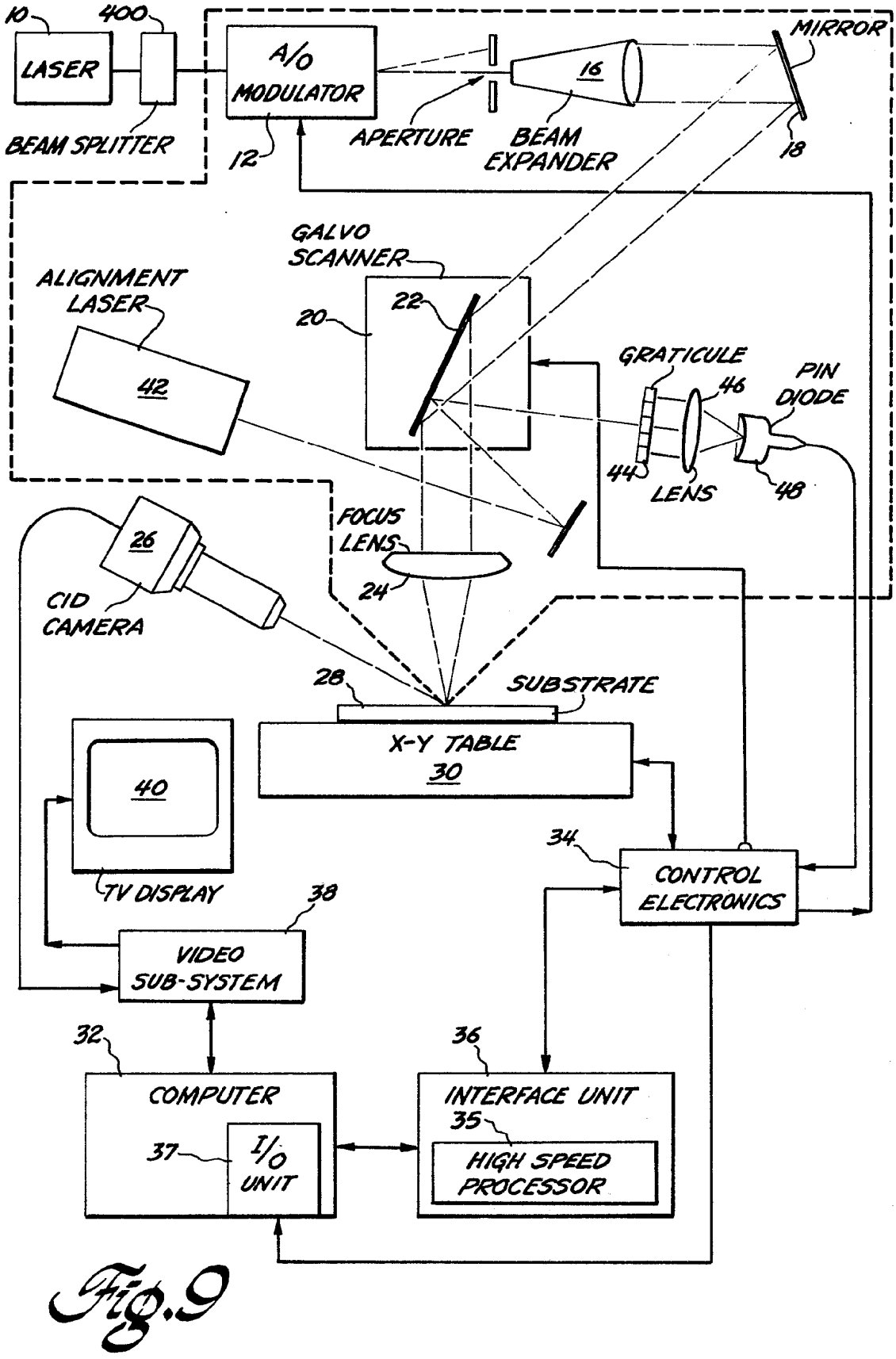


Fig. 8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LASER
BEAM SPLITTER
A/O
MODULATOR
12
APERTURE
16
BEAM
EXPANDER
MIRROR
18
GALVO
SCANNER
20
22
ALIGNMENT
LASER
42
GRATICULE
46
PIN
DIODE
44
LENS
48
FOCUS
LENS
24
26
CID
CAMERA
28
SUBSTRATE
X-Y TABLE
30
40
TV DISPLAY
34
CONTROL
ELECTRONICS
38
VIDEO
SUB-SYSTEM
32
COMPUTER
37
I/O
UNIT
36
INTERFACE UNIT
35
HIGH SPEED
PROCESSOR

Fig. 9